

1 CLAIMS

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We claim:

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1. A trench DMOS transistor cell comprising:

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a substrate of semiconductor material of heavily

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doped first electrical conductivity type;

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a first covering layer of semiconductor material

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of first conductivity type lying on the substrate;

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a second covering layer of semiconductor material

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of second electrical conductivity type lying on the

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first covering layer and having a bottom surface;

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a third covering layer of semiconductor material

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of heavily doped first conductivity type and having a

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top surface and partly lying over the second covering

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layer, where a portion of the second covering layer is

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heavily doped and this portion extends vertically

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upward through a portion of the third covering layer to

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the top surface thereof;

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a trench having a bottom surface and side surfaces

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and extending vertically downward from the top surface

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of the third covering layer through the third and

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second covering layers and through a portion of the

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first covering layer, where the bottom surface of the

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trench lies above a lowest part of the bottom surface

26

of the second covering layer;

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electrically conducting semiconductor material

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positioned within the trench;

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a layer of oxide positioned within the trench

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between the electrically conducting semiconductor

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material and the bottom and side surfaces of the

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trench; and

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three electrodes electrically coupled to the

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electrically conducting material, to the third covering

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layer and to the substrate, respectively.

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2. A trench DMOS transistor cell comprising:

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a substrate of semiconductor material of heavily

1 doped first electrical conductivity type having a top
2 surface;

3 a first covering layer of semiconductor material
4 of first conductivity type having a top surface and
5 being contiguous to and overlying the substrate top
6 surface;

7 a second covering layer of semiconductor material
8 of second electrical conductivity type having a top
9 surface and being contiguous to the top surface of the
10 first covering layer and extending vertically downward
11 from the top surface of the first covering layer into
12 an upper portion of the first covering layer;

13 a third covering layer of semiconductor material
14 of heavily doped first conductivity type having a top
15 surface and being contiguous to and partly overlying
16 the top surface of the second covering layer, where a
17 portion of the second covering layer is heavily doped
18 and this portion extends vertically upward through the
19 third covering layer to the top surface thereof and
20 forms an exposed pattern of the second covering layer
21 adjacent in the top surface of the third covering
22 layer, where the maximum depth of the heavily doped
23 portion of the second covering layer relative to the
24 top surface of the third covering layer is a
25 predetermined number d_1 , and where the depth of the top
26 surface of the substrate at a position that underlies
27 the position of maximum depth of the heavily doped
28 portion of the second covering layer is a second
29 predetermined number d_2 ;

30 a trench having side surfaces and bottom surfaces
31 and extending vertically downward from the top surface
32 of the third covering layer through the third covering
33 layer, through the second covering layer and through a
34 portion of, but not all of, the first covering layer,
35 the trench bottom surface having a maximum depth
36 relative to the top surface of the third covering layer
37 equal to a third predetermined number d_3 where $d_3 < d_1$,
38 where the trench in horizontal cross section is

1 approximately a polygonal stripe with stripe width
2 approximately equal to a fourth predetermined number b,
3 and where this polygonal stripe laterally surrounds and
4 is spaced apart from the exposed pattern of the second
5 covering layer at the top surface of the third covering
6 layer;

7 a layer of oxide, positioned within the trench and
8 contiguous to the bottom surfaces and side surfaces of
9 the trench so that a portion of, but not all of, the
10 trench is filled with this oxide layer;

11 electrically conducting semiconductor material,
12 having resistivity of approximately one ohm-cm, that is
13 contiguous to the oxide layer and positioned within the
14 trench so that this electrically conducting material is
15 spaced apart from the side walls and the bottom walls
16 of the trench by the oxide layer; and

17 three electrodes that are electrically coupled to
18 the electrically conducting semiconductor material in
19 the trench, to the third covering layer and to the
20 substrate, respectively.

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22 3. A cell according to Claim 2, wherein said
23 substrate has a doping concentration of at least 10^{18}cm^{-3} .

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25 4. A cell according to Claim 2, wherein said first
26 covering layer has a doping concentration in the range of
27 $10^{15}-10^{17}\text{cm}^{-3}$.

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29 5. A cell according to Claim 2, wherein said
30 vertically extending portion of said second covering layer
31 has a doping concentration of at least 10^{18}cm^{-3} .

32
33 6. A cell according to Claim 2, wherein said third
34 covering layer has a doping concentration at the top surface
35 of at least $5 \times 10^{19}\text{cm}^{-3}$.

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37 7. A cell according to Claim 2, wherein the shape of
38 said polygonal stripe is drawn from the class consisting of

1 a hexagon, a circle and an oval.

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3 8. A cell according to Claim 2, wherein said second
4 covering layer exposed pattern has the shape of a hexagon.

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6 9. A cell according to Claim 2, further comprising a
7 second oxide layer contiguous to said electrically
8 conducting trench material within said trench.

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10 10. A cell according to Claim 7, further comprising a
11 trench-filling semiconductor material that is contiguous to
12 said second oxide layer within said trench and that
13 substantially fills the remainder of said trench.

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15 11. A cell according to Claim 2, wherein the
16 difference $d_1 - d_3$ between said predetermined numbers d_1 and
17 d_3 is $0.5\mu\text{m}$ or greater.

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19 12. A cell according to Claim 2, wherein the
20 difference $d_2 - d_1$ between said predetermined numbers d_2 and
21 d_1 is $1.25\mu\text{m}$ or less.

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23 13. A cell according to Claim 2, wherein said trench
24 oxide layer has a thickness on said side surfaces and said
25 bottom surfaces of said trench that lies in the range $0.1 -$
26 $0.2\mu\text{m}$.

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28 14. A method for providing a trench DMOS transistor
29 cell, the method comprising the steps of:

30 providing a substrate of semiconductor material of
31 heavily doped first electrical conductivity type having
32 a top surface;

33 providing a first covering layer of semiconductor
34 material of first conductivity type having a top
35 surface and being contiguous to and overlying the
36 substrate top surface;

37 providing a second covering layer of semiconductor
38 material of second electrical conductivity type having

1 a top surface and being contiguous to the top surface
2 of the first covering layer and extending vertically
3 downward from the top surface of the first covering
4 layer into an upper portion of the first covering
5 layer;

6 providing a third covering layer of semiconductor
7 material of heavily doped first conductivity type
8 having a top surface and being contiguous to and partly
9 overlying the top surface of the second covering layer,
10 where a portion of the second covering layer is heavily
11 doped and this portion extends vertically upward
12 through the third covering layer to the top surface
13 thereof and forms an exposed pattern of the second
14 covering layer in the top surface of the third covering
15 layer, and where the maximum depth of the heavily doped
16 portion of the second covering layer relative to the
17 top surface of the third covering layer is a
18 predetermined number d_1 ;

19 providing a trench having side walls and bottom
20 walls and extending vertically downward from the top
21 surface of the third covering layer through the third
22 and second covering layers and through a portion of,
23 but not all of, the first covering layer, where the
24 trench has a maximum depth relative to the top surface
25 of the third covering layer equal to a second
26 predetermined number d_2 and d_2 is less than d_1 , where
27 the trench in horizontal cross section is approximately
28 a polygonal stripe, and where this polygonal stripe
29 laterally surrounds and is spaced apart from the
30 exposed pattern of the second covering layer at the top
31 surface of the third covering layer;

32 providing a layer of oxide, positioned within the
33 trench and contiguous to the bottom walls and side
34 walls of the trench so that a portions of, but not all
35 of, the trench is filled with this oxide layer;

36 providing electrically conducting semiconductor
37 material, contiguous to the oxide layer and positioned
38 within the trench so that the oxide layer lies between

1 the electrically conducting semiconductor material and
2 the bottom and side walls of the trench; and
3 providing three electrodes that are electrically
4 coupled to the electrically conducting semiconductor
5 material in the trench, to the second covering layer
6 and to the substrate, respectively.
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8 15. The method according to Claim 14, further
9 comprising the step of providing said trench with rounded
10 corners of oxidized material, where said bottom surfaces and
11 said side surfaces of said trench meet and where said side
12 surfaces of said trench meet said top surface of said third
13 covering layer and where said side surfaces of said trench
14 meet with one another.
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16 16. The method according to Claim 14, wherein said
17 steps of providing said third covering layer and providing
18 said trench include the step of choosing the difference
19 $d_1 - d_2$ of said first and second predetermined numbers d_1 and
20 d_2 as 0.5 μm or greater.
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